Novel Addressable Test Structure for Detecting Soft Failure of Resistive Elements when Developing Manufacturing Procedures

Shingo Sato, *Member, IEEE*, and Yasuhisa Omura, *Fellow, IEEE*

***Abstract*—A novel addressable test structure for detecting soft failures of resistive elements is proposed. Its architecture is much simpler than that of previous works, but all functions needed to analyze the electrical properties of detected failures, for example the aging test with overcurrent, can be realized within the architecture. This makes it more powerful than previous designs. Since the addressable test structure proposed here also has a smaller footprint, it can realize cost effective evaluations.**

***Index Terms*—addressable test structure, failure, soft open and short, variation, yield.**

I. Introduction

THE technology node of the CMOS semiconductor process has already been aggressively scaled [1], [2]. More effective techniques for managing and monitoring the yield of the semiconductor manufacturing process are necessary given the sheer number of electrical elements present in the latest integrated circuits.

One of the most promising and interesting techniques for managing yield is to utilize the addressable test structure (ATS). In ATS, many electrical elements placed in a lattice are addressed by peripheral circuits like counters or shift registers. and are measured one by one. The advantage of this technique is its ability to evaluate the variation in electrical properties caused by the manufacturing process. In addition, failures with high/low resistances, not fully open/shorts, can be detected thanks to the failure detection resolution and the number of devices under test. Unfortunately, this technique has the drawback of measurement times longer than those of simple test structures like Kelvin resistance measurement. Studies to date have tried to optimize the trade-offs involved.

Various kinds of ATSs have already been proposed for measuring the electrical properties of elements like transistors [3], contacts [4], capacitors [5], and resistors [6]. A recently proposed circuit architecture to analyze the soft failure of resistive elements was based on circuit simulations [7]. This paper reports measured results from fabricated chips.

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II. Details of Architecture and Measurement

In this section, an architecture of the ATS, measurement system and measurement flow for detecting the failures are described.

A. Chip Design

Fig. 1 shows the diagram of the structure as a chip. It consists of main part of the ATS, where unit cells consisting of resistive elements are placed in a lattice, addressing circuits for horizontal and vertical lines, which use inputs of 'init' and 'clk' for initializing and changing the address of the ATS, and the 4 to 16 decoder, which has the input of 'sel<0:3>' for selecting the location of the resistive element in the unit cell. The unit cells are addressed by column and row decoders designed with the ring counter and the shift register. The last output from the ring counter of the column decoder is used as an input pulse to the shift resister of the row decoder. Firstly, the address information of the unit cells is initialized by input pulse of 'init'. Then, the outputs from ring counter are shifted for column direction by input pulse of 'clk'. When the number of the input pulse to column decoder exceeds the maximum column number, the outputs from the row decoder are shifted for row direction.

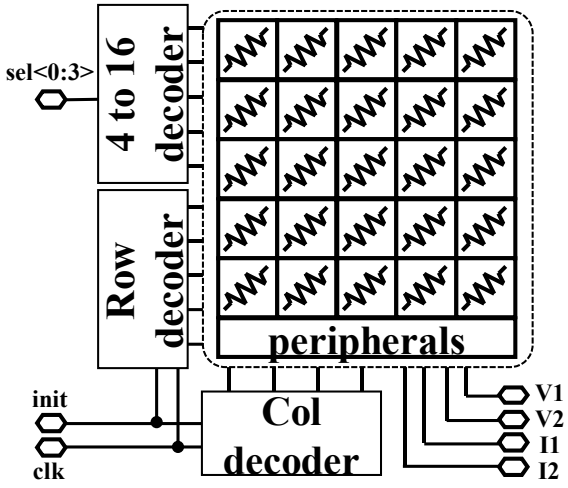


Fig. 1. The chip diagram proposed in this work. It consists of main part of the ATS, addressing circuit and 4 to 16 decoder. The signals of 'init' and 'clk' are inputs for initializing and changing the address of ATS, respectively. The signals of 'sel<0:3>' are the input to 4 to 16 decoder.

The crossing point of the outputs from row and column decoders is selected and the resistive element of selected unit cell is evaluated.

Fig. 2 shows the circuit schematic of the unit cell. 'I1', 'I2', 'V1' and 'V2' are Input/Output (I/O) of bus for forcing/sensing current/voltage signals; they are connected to same terminals via peripherals drawn in Fig. 1. The resistance of resistive element R_{DUT} is calculated by using the standard Ohm's law with current loaded between 'I1' and 'I2' and potentials measured on both sides of R_{DUT}, 'V1' and 'V2'. This unit cell has a standard Kelvin structure to eliminate the parasitic resistance and the terminals to sense local potentials of the resistive element, whose gates are controlled by the output of the 4 to 16 decoder, 'g<0:15>'. The pass gates passing through 'I1' and 'I2' must be designed with gate width large enough to suppress the voltage drop when large currents are used. Since this unit cell has a symmetrical structure, bidirectional current can be applied to each resistive element. The pass gates connected to 'V1' and 'V2' consist of p-ch and n-ch transistors in this study.

The number of pads used for a chip is 2 for address, 4 for changing the location sensed, 4 for measuring DUT, 2 for supplying nominal voltages; 12 in total.

This ATS is implemented using 3.3V I/O transistors of 65nm SOI CMOS technology and two Cu metal layers. The layout area of the unit cell is 16.47×23.64um^2. The layout area of two unit cells is equivalent to that of "Block" in the previous work [8] but is 12% smaller. The total layout area, which includes the peripheral digital circuit and the unit cell arrays of 33×33, is about 1.5×1.0mm^2.

B. Measurement System

Fig. 3 shows a schematic of the measurement system used in this paper. The data acquisition system consisted of an 18bit precision analog to digital converter (ADC) board and a Xilinx Artix-7 evaluation board designed by Tokushu Denshi Kairo Incorporated. Nominal voltage is supplied by a dc voltage source of Matsusada Precision Incorporated. The impressed current is provided by a KEITHLEY 2450 Source Meter.

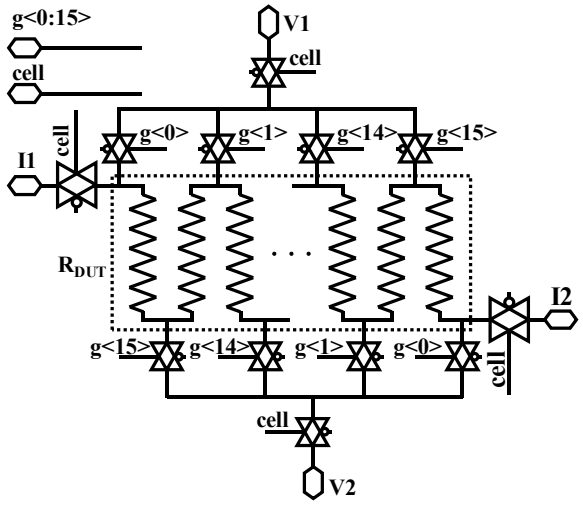


Fig. 2. The circuit schematic of the unit cell. The resistance of R_{DUT} is calculated by using standard Ohm's law with impressed current between 'I1' and 'I2' and measured potentials for both side of R_{DUT}, 'V1' and 'V2'.

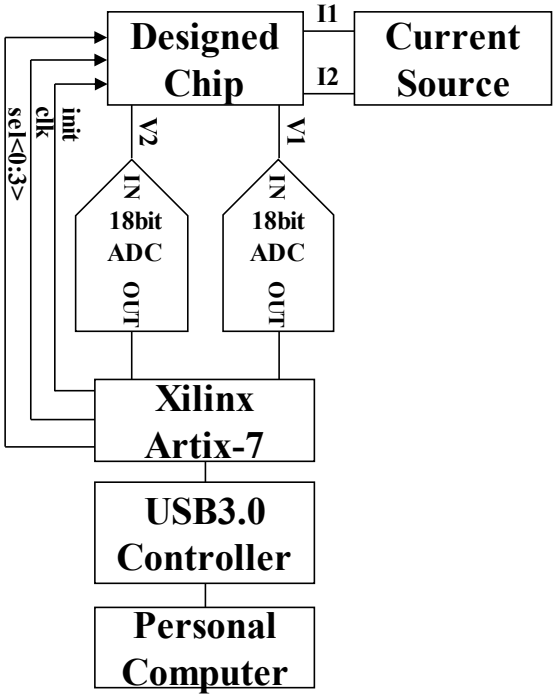


Fig. 3. The schematic of the measurement system used in this paper. The voltages of 'V1' and 'V2' are digitized by 18bit ADC. The digitized data are collected to personal computer via FPGA and USB controller.

The pulses and four bit binary signal output from General-Purpose I/O of Artix-7 evaluation board are input to 'init', 'clk' and 'sel<0:3>'. The current between 'I1' and 'I2' is loaded via the source meter. The voltages 'V1' and 'V2' are measured by the ADC board.

C. Measurement Flow

Measurement flow for detecting failures almost matches that of the previous work [8]. First, all the unit cells in the ATS are measured with logic signal 'sel<0:3>' of '0000'. Then, global variation is removed by filtering the measured resistances. Finally, all the divided resistors inside the unit cell, which are suspected as exhibiting failure from the tail of the distribution, are measured by changing the logic signal 'sel<0:3>'.

The proposed ATS does not require a peripheral circuit to switch series resistance mode to unit resistance mode, which is required by the previous work [8], and the resolution to detect the failure can be easily adjusted by changing the logic signal 'sel<0:3>' in the first measurement. Accordingly, proposed ATS is sufficiently flexible to support any stage of the process development.

III. Measurement Results

This section details results on the measurement accuracy and failure detection. The resistive elements measured are the 1st via chain, the via chain stacked from the 1st to 4th via and the poly resistor. The current loaded onto the resistive elements was adjusted in the range of 1.0uA to 2.0mA to obtain reasonable voltage drops between 'I1' and 'I2' terminals.

A. Measurement accuracy

Fig. 4 plots the correlation of the resistance value measured with the proposed ATS against the resistance value measured with the standard Kelvin test structure having the same layout. The correlation is good over a wide range of resistance values, from 10Ω to 1MΩ.

Fig. 5 plots the cumulative probability of the measured resistance values as a parameter of the input signal label for the 4 to 16 decoder 'sel<0:3>'. Since the cumulative probability plot directly shows the variation of the measured result, electrical characteristics are easily examined. The measured resistance values with each logic signal are modulated since the address of the resistive element inside the unit cell is changed as shown in Fig. 2 and the median value of measured resistance has a linear dependence since the resistive element inside the unit cell are equally divided.

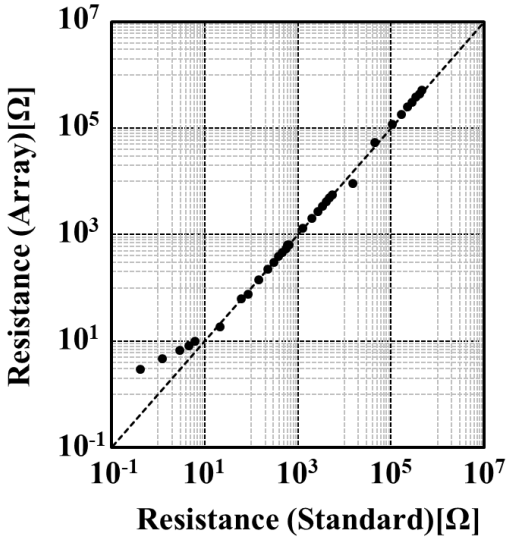


Fig.4. Correlation plot of the resistance determined with proposed ATS against that with standard Kelvin test structure. Good correlation for wide range of resistance values from 10Ω to 1MΩ can be observed.

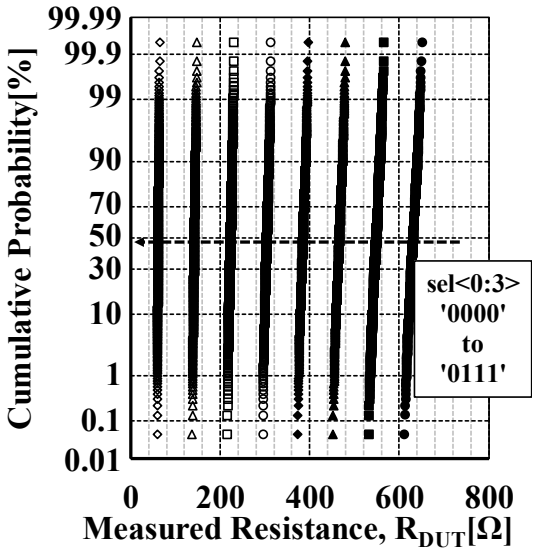
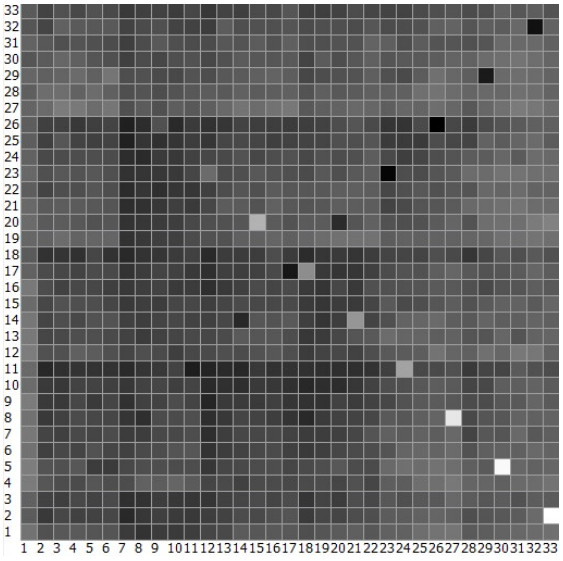


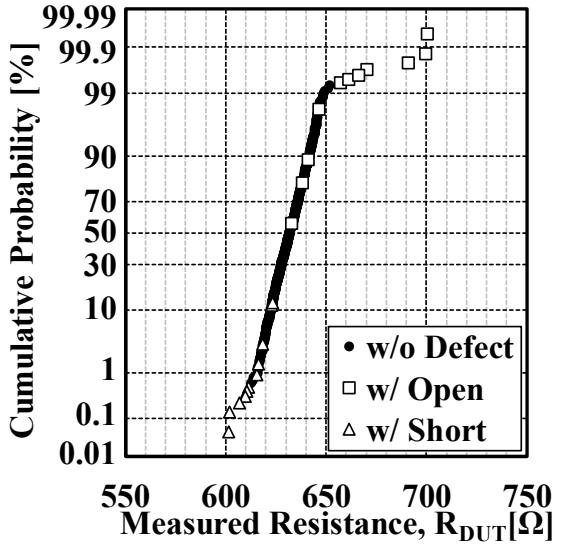
Fig.5. Cumulative probability of the resistance measured with different input signal 'sel<0:3>' from '0000' to '0111'. The median values of the resistance are proportional for each logic signal.

B. Detection of the Failures

Fig. 6(a) and 6(b) show the bitmap image and cumulative probability of the 1st via chain resistance values measured with the proposed ATS; 'sel<0:3>' was set to '0000'. Dark hues indicate low resistances. Programmed defects, which have slightly higher or lower resistance than reference resistance value, were implemented on a diagonal line of the array every third unit cell. More specifically, programmed open/short defects were implemented at the addresses of (3+3n, 32-3n) / (2+3n, 2+3n) using integer 'n' from 0 to 10. The resistance value difference between programmed defect and reference resistive element increases to the right in the figure. The standard deviation of the measured resistances after excluding the programmed defects is 7.03Ω; this includes the measurement error induced by peripheral circuit and the global



(a)



(b)

Fig.6. (a) Bitmap image of the resistances measured with proposed ATS. Programmed defects are implemented on a diagonal line. The darker the colored pixel is, the lower its resistance is. (b) Cumulative probability as a function of measured resistance

variation induced by manufacturing process of resistive elements.

The operations for removing these variations were applied to the bitmap image of the measured resistance values. There are two operations, 'Mismatch' and 'High Pass Filter (HPF)' [7]. Operation 'Mismatch' differentiates the nearest neighbor horizontal pixels. Operation 'HPF' subtracts the median resistance value of the nearest nine neighbor pixels from the center one. Fig. 7 plots the cumulative probability of the resistance value after these two operations. The standard deviation for 'Mismatch' and 'HPF' are 4.20Ω and 3.13Ω. The ratio of the standard deviation between both operations (~1.34) is almost equal to the theoretical prediction (~1.41) [7]. The two operations swept the programmed defect cells from the vicinity of the center of the main distribution and some of them are clearly recognized as defective, as significant improvement over Fig. 6. We can see that the global variation is successfully removed from the measurement results with above operations. These results indicate the importance of the operation to remove global variation when the soft failures are manufactured in the wafer process. In case of 'Mismatch', the open and short soft failures cannot be classified into each category of the failure in the measurement sequence since those are output with mixed states around the tail of the cumulative probability. On the other hand, the failures can be classified into each category in case of 'HPF' easily since open and short ones are output for positive and negative tail of the cumulative probability.

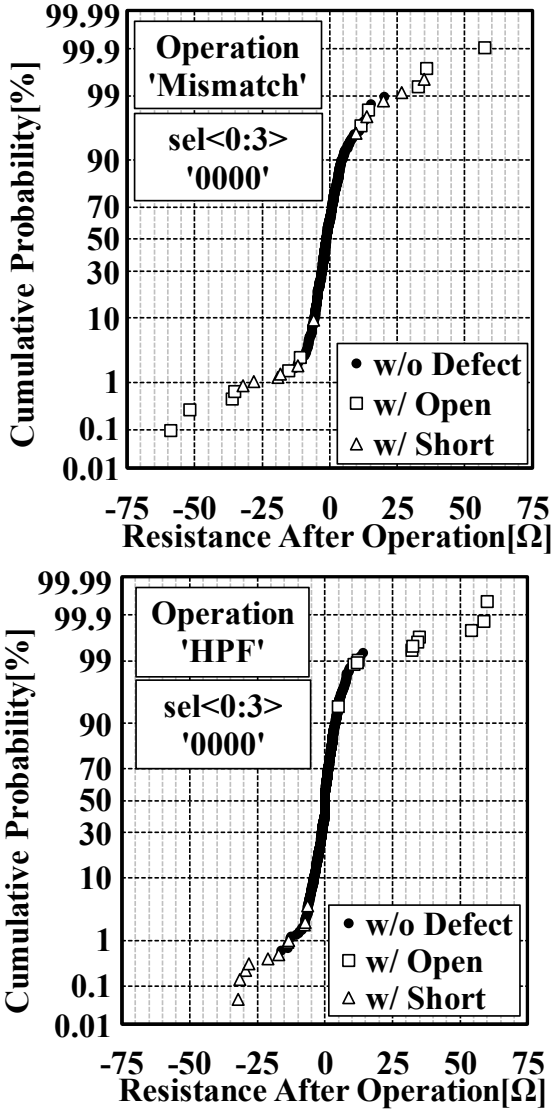


Fig. 7. Cumulative probability as a function of the resistance after operations to remove global variation. The signal 'sel<0:3>' are set to be '0000'.

Fig. 8 indicates the cumulative probability as a function of the resistance value after the operation 'HPF' measured with the signal 'sel<0:3>' of '0011'. Programmed open defects are not included in this result because it is implemented at outermost divided resistor drawn in Fig. 2. The six and eight programmed defects can be identified as the candidate of the failure in Fig. 7 and 8 because those become the tail of the distribution. The resolution of detecting failures, that is determined by the ratio of the defect resistance value and the local variation of values of the resistive elements, can be adjusted by changing the signal 'sel<0:3>', which adjusts the number of the resistive elements in the measurement as shown in Fig. 7 and 8.

The measurement to find the specific location of the failure is performed after a cell is identified as having a possible failure in Fig. 7. As an example, the measurement result as a function of the resistance for all divided resistors inside the suspected cell is shown in Fig. 9. The divided resistor whose resistance is four times larger than the average resistance was successfully detected. Although the failure detected in this study is intentionally implemented, we will be able to detect soft failures even in actual situations like process development. Since this measurement sequence indicates the specific location, we do not need to use other techniques like voltage contrast to identify the location of the failure inside the cell. We can easily investigate the issue by physical analysis techniques like Transmission-Electron-Microscopy (TEM) [8].

One of the most interesting problems for engineers engaging

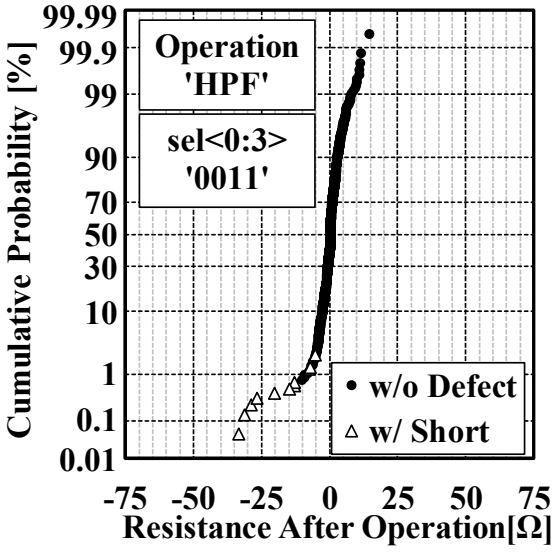


Fig. 8. Cumulative probability as a function of the resistance after operations to remove global variation. The signal 'sel<0:3>' is set to be '0011'.

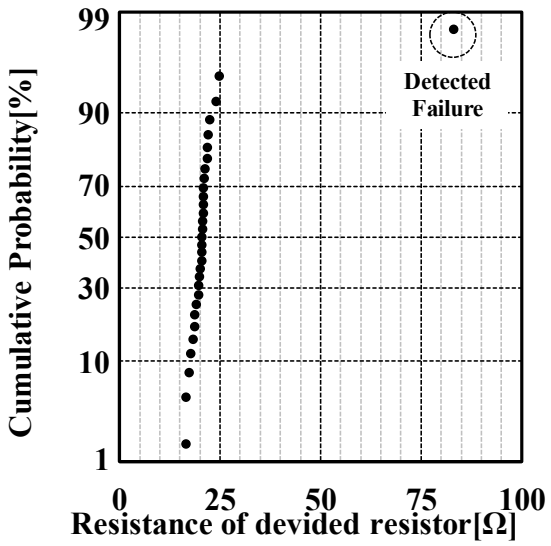


Fig. 9. Cumulative probability of the resistance for all divided resistors inside the suspect cell.

in the manufacturing process is whether detected soft failures will worsen after shipping or not. If the problem worsens, the product chip shipped after electrical testing may become a failed market product. To confirm the possibility of the soft failure worsening, the function of applying overcurrent to it is required [9]. Fig. 10 indicates the correlation plot of the resistance with standard measurement against overcurrent measurement. The current density of the overcurrent measurement is 10MA/cm^2 as used in a recent migration test [10]. Good correlation between the resistance measured with standard and overcurrent measurement is found. The maximum error between overcurrent and standard measurement is below 0.4%. Combining overcurrent with high temperatures will yield aging tests that offer superior detection rates.

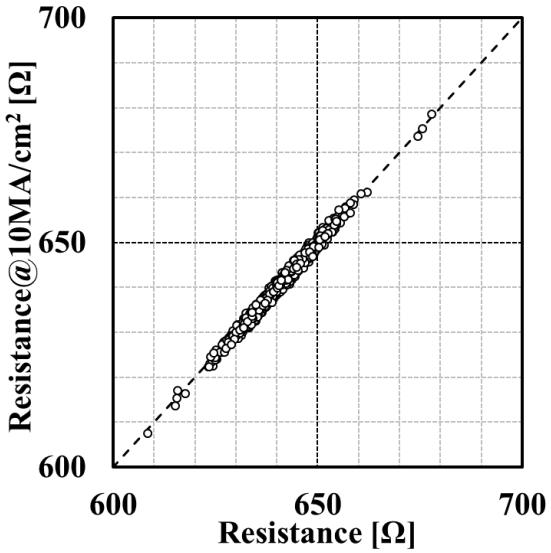


Fig. 10. Correlation plot of resistance with standard measurement versus overcurrent measurement shows excellent correlation.

IV. Conclusion

A novel ATS for detecting soft failures of resistive elements was proposed in this paper. The performance of the proposal in terms of measurement accuracy and the detection of failures was demonstrated and its viability was clarified. The architecture of the proposed ATS is very simple but it offers very powerful functions such as adjusting the resolution for detecting failures, aging tests with overcurrent loading to detect immanent failures. Since the layout area is reduced by 88% compared to previous work, the proposed ATS greatly reduces overheads.

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