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Compact Equivalent-Circuit Model for Snap-Back Phenomena in Ultra-Thin SOI MOSFET's and Practical Guideline for ESD-Protection Device Design

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Abstract

This paper proposes a compact equivalent-circuit model for the snap-back phenomenon in ultra-thin SOI MOSFET's. The model can be used in simulations of I/O circuits with ESD-protection devices. The model is more simple than past models, but it successfully reproduces the snap-back response. With the aid of many simulations, we propose a guideline for snap-back SOI MOSFET device design. Useful parameter-sensitivity equations for device characteristics are given for practical device designs.

Key words: SOI MOSFET, snap-back, parasitic bipolar action, electrostatic discharge, equivalent circuit model

1. Introduction

Electrostatic discharge (ESD) phenomena continue to be an issue because of technology scaling, RF application requirements, and increasing customer expectations. Concurrently, ESD networks, technologies and device/circuit design practices are constantly undergoing both evolutionary and revolutionary changes[1, 2]. The current levels of ESD events are generally in excess of 1 A for durations of from a few nanoseconds to 100 ns, and can severely damage integrated circuits. The most sensitive areas of integrated circuits are the devices directly connected to the bond pads. In order to protect the input/output (I/O) buffers from ESD stress, protection circuits that act as voltage clamps and current shunts are placed in parallel with the I/O circuits. An ESD protection circuit should turn on during the ESD event and clamp the excess voltage before the I/O buffer is damaged or worn out. In other words, engineers must predict the possibility of ESD damage in protection circuits and design robust device structures[3, 4].

The design and optimization of ESD protection circuits is greatly enhanced by the ability to perform circuit-level simulations of the protection circuits and the I/O buffers. Most available simulations do not reliably cover the high current region of circuit operation, but provide an approximate analysis of circuit behavior under ESD events[5, 6]. The growing use of MOS-based protection circuits[5, 7], and the integration of protection circuits with internal circuitry[6, 8], has led to a need for simulations that are able to more accurately reproduce the behavior of a circuit under ESD events.

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In this paper, we propose an equivalent circuit model for snap-back MOSFET's for ESD Protection circuits on silicon-on-insulator (SOI) substrates[9, 10]. With the aid of a device simulator (*ISETCAD-DESISS*[11]), the proposed equivalent circuit model is extensively examined by greatly varying many device parameters. Finally, we propose parameter-sensitivity equations that cover the gain of a parasitic bipolar transistor, the breakdown voltage (turn-on voltage), and the holding voltage, all of which are required in designing an effective device structure.

2. Experimental Results of Snap-back Operation

Before considering the equivalent circuit model, we examined the fundamental potential of the device simulator *ISE-DESSIS*[11]. Experimental results of snap-back operation in 50-nm-thick SOI MOSFET with 1-μm-long channel are shown in Fig. 1; the channel length (L_{eff}) is 0.8μm, the gate oxide layer thickness (t_{ox}) is 7 nm, the SOI layer thickness (t_{si}) is 50 nm, the buried oxide layer thickness (t_{BOX}) is 80 nm, the p-type body-doping concentration (N_A) is 5×10^{17}cm^{-3}, and the n-type doping concentration of gate poly-Si and source/drain region is 1×10^{20}cm^{-3}. Since the device works as a fully-depleted SOI MOSFET due to the positive fixed charges in the buried oxide layer, it does not exhibit snap-back operation at zero-substrate bias. Accordingly, we applied -10V to the substrate against the source terminal. We note that the breakdown voltage (V_{BD}) is 3.6 V and holding voltage (V_{SB}) is 2.9 V.

We also simulated the snap-back characteristic of an SOI MOSFET having device parameters identical to the actual device parameters, but no account of fixed charges in the buried oxide layer was taken: the fully-depleted operation does not occur. The device structure assumed here is shown in Fig. 2. It is assumed that the gate voltage (V_G), the source voltage (V_S), and the substrate voltage (V_{SUB}) are all 0 V; the ramping rate of current applied to the drain terminal is 50 mA/ms; and the maximal voltage of 10 V is applied to the drain terminal because the holding voltage is about 4 V. Such a slow current ramping rate was

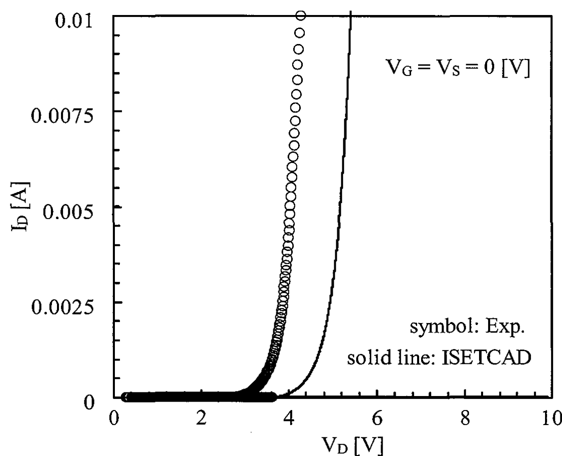

Fig.1 Snap-back operation of ultra-thin SOI MOSFET. Experimental result is shown with the simulation result (*ISE-DESSIS*). Substrate voltage (V_{sub}) is $-$ 10 V in the experiment and 0 V in the simulation.

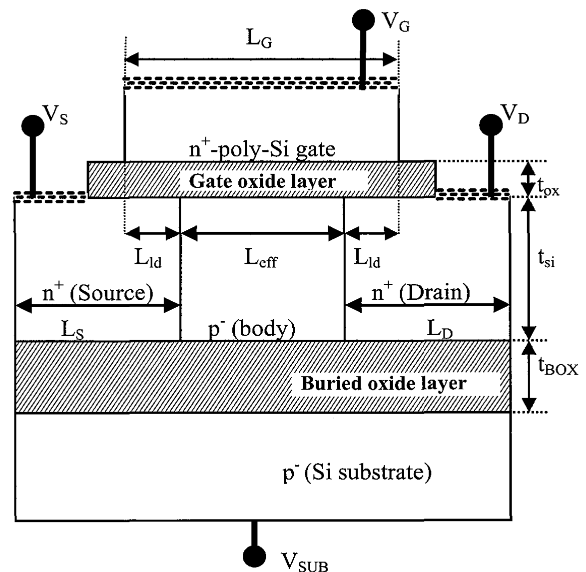

Fig. 2 Schematic of SOI MOSFET device structure simulated.

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selected with a view to ease of measurement. However, the ramping rate is still fast compared to the measurement condition. When we assumed a slower ramping rate, the simulations took too long. Since the purpose of this simulation is to show the capability of *DESSIS*, we have shown only feasible simulation results in Fig. 1. We used the hydrodynamic transport model in device simulations, because a device experiencing snap-back has both high current and high heat flow. It is assumed that the carrier lifetime of electrons is 10μs and that of holes is 3μs. Here, we used the Masetti model[12], the Lombardi model[13], and the Canali model[14] for carrier mobility models. We also assumed the Shockley-Read-Hall type lifetime model proposed by Fossum[15], the Auger recombination model described in[11], and the band-gap narrowing model [16]. We can see that the simulation results broadly reproduce the experimental results. So, we can conclude the models implemented in the simulator are acceptable for practical use.

3. Device Structure and Device Parameters

In the following simulations, we also assumed the SOI MOSFET structure shown in Fig. 2. Basic device parameters are shown in Table I. It is assumed that the gate voltage (V_G), the source voltage (V_S) and the substrate voltage (V_{SUB}) are all 0 V, and that the ramping rate of the current applied to the drain terminal is 5 mA/ns. It is also assumed that the maximal voltage of 12 V is applied to the drain terminal because the breakdown voltage (turn-on voltage) is about 7 V in *DESSIS* simulations. This rather rapid ramping rate was selected with a view to observing ESD events. We used the hydrodynamic transport model in device simulations because actual devices exhibit high currents with heat flow. In addition, we varied device parameters within the ranges shown in Table II. From the simulations, we derived three parameter-sensitivity equations for device design.

Table I. Basic device parameters in simulations

Parameters	Values [unit]
Channel length (L_{eff})	0.15 [μm]
Gate width (W)	1.0 [μm]
Gate oxide thickness (t_{ox})	3.5 [nm]
SOI layer thickness (t_{si})	0.1 [μm]
Buried oxide layer thickness (t_{BOX})	0.1 [μm]
SOI doping conc. (N_A)	9×10^{17} [cm^{-3}]
Lateral diffusion length (L_{ld})	15 [nm]
Substrate doping conc. (N_{sub})	1×10^{15} [cm^{-3}]
Source/Drain doping conc. ($N_{S/D}$)	1×10^{20} [cm^{-3}]
Gate poly-Si doping conc. (N_G)	1×10^{20} [cm^{-3}]
Source/Drain length ($L_{S/D}$)	0.555 [μm]
Minority carrier lifetime	10 (for electrons) [μs], 3 (for holes) [μs]

Table II. Variable range of device parameters in simulations

Parameters	Values [unit]
Channel length (L_{eff})	0.07 – 0.27 [μm]
Gate width (W)	0.1 – 10 [μm]
Gate oxide thickness (t_{ox})	1.5 – 10 [nm]
SOI layer thickness (t_{si})	0.1 – 0.5 [μm]
Buried oxide layer thickness (t_{BOX})	0.05 – 0.3 [μm]
SOI doping conc. (N_A)	$2\times10^{17}-5\times10^{18}$ [cm^{-3}]
Lateral diffusion length (L_{ld})	15 – 60 [nm]
Source/Drain length ($L_{S/D}$)	0.4 – 2.9 [μm]

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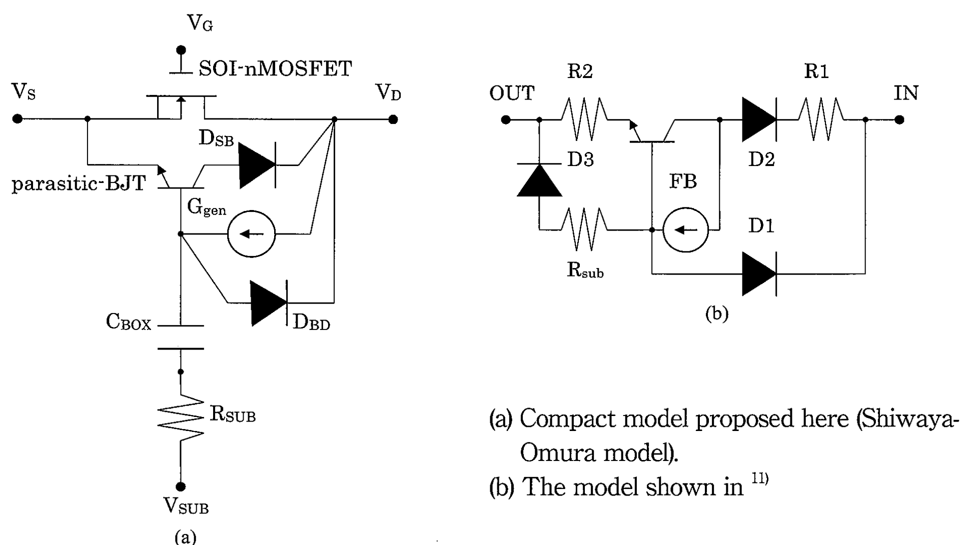
4. Results and Discussion

A. Equivalent circuit model

We investigated past equivalent circuit models[17-21]. Generally speaking, past models use many empirically-derived fitting parameters, which have no physical basis, depending on device parameters. For engineers, parameters for the equivalent circuit model should be actual physical parameters. Taking this as our guideline, we proposed the equivalent circuit model shown in Fig. 3(a). One of the past models is also shown in Fig. 3(b)[20] for comparison. We tried to minimize the number of circuit components, as follows: (i) parasitic resistances, such as *R1* and *R2* in Fig. 3(a), were removed and incorporated into the passive components of parasitic bipolar transistor; (ii) diode “*D2* was replaced with “D_{SB} in order to ensure the holding voltage (V_{SB}) based on actual physical parameters; (iii) diode “*D1* was replaced with “D_{BD} to ensure the breakdown voltage based on actual physical parameters; and (iv) diode “*D3* was removed and its role incorporated into the parasitic bipolar transistor.



(a) Compact model proposed here (Shiwaya-Omura model).
(b) The model shown in [11]

Fig. 3 Equivalent circuit model for SPICE simulations.

B. Confirming the potential of the proposed model

We assessed the potential of the proposed model (Fig. 3(a)). Typical simulation results are shown in Figs. 4 to 7, where circuit simulation results are compared to device simulation results. Fig. 4 shows the drain current dependence on drain voltage with the parameter of channel length (L_{eff}); Fig. 5 shows the drain current dependence on drain voltage with the parameter of SOI layer thickness (t_{si}); Fig. 6 shows the drain current dependence on drain voltage with the parameter of body-doping concentration (N_A); and Fig. 7 shows the drain current dependence on drain voltage with the parameter of lateral diffusion length (L_{ld}). Drain current dependence on drain current with the parameter of t_{BOX} or t_{ox} is not shown because the drain current is not so sensitive to them. Device simulation results are denoted by symbols, while circuit simulation results are denoted by solid lines. It is clear that the proposed model successfully reproduces the device simulation results.

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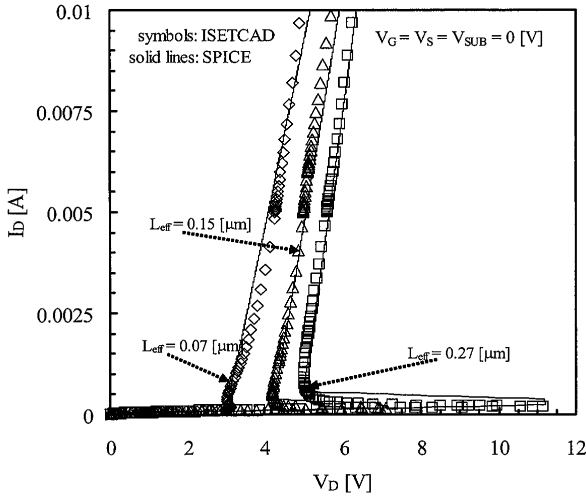

Fig. 4 Drain current dependence on drain voltage for various channel lengths (L_{eff}).

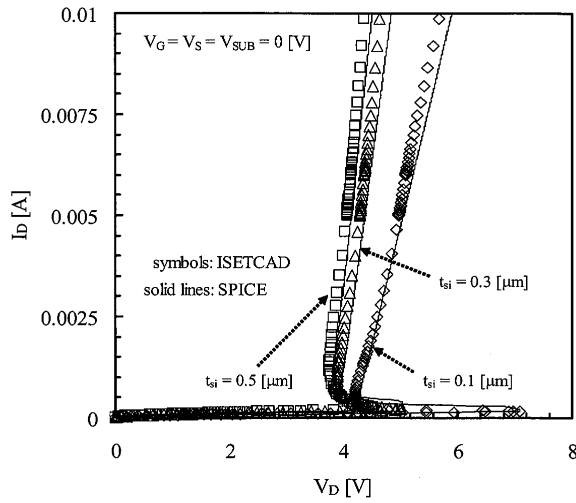

Fig. 5 Drain current dependence on drain voltage for various SOI layer thicknesses (t_{si})

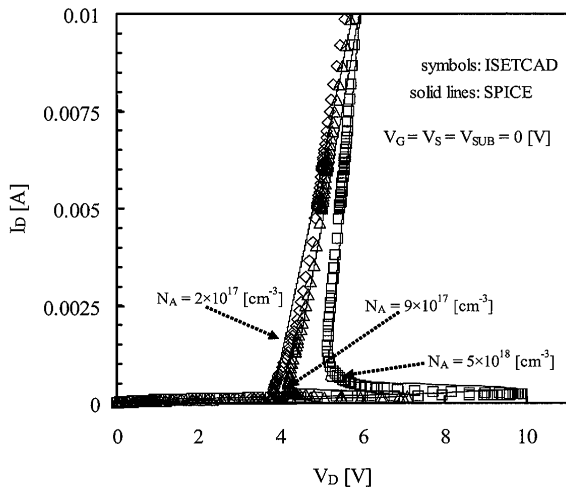

Fig. 6 Drain current dependence on drain voltage for various body-doping concentrations (N_A)

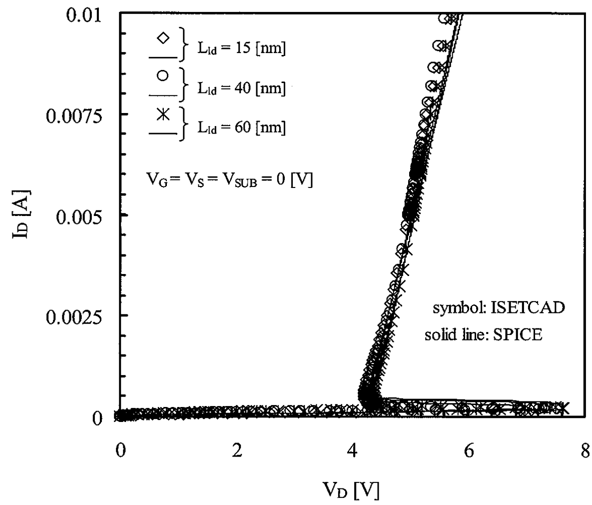

Fig. 7 Drain current dependence on drain voltage for various lateral diffusion lengths (L_{ld})

C. Parameter-sensitivity equations for practical device design

From the above simulation results, we derived several equations that can accurately express device characteristics, and so yield better designs. These equations can be used to design snap-back SOI MOSFET's for ESD protection circuits using the model shown in Fig. 3(a).

(i) Saturation current (IS) of diodes "D_{SB} and "D_{BD} is defined as

$$IS = A\,\frac{qD_n n_i^2}{L_{eff} N_A}, \tag{1}$$

where A is the junction area, and the other parameters have the conventional meaning.

(ii) Constant current source (I_{gen}) is defined with

$$I_{gen} = gain \cdot (I_{DS} + I_C) = (M-1)\,(I_{DS} + I_C)\,, \tag{2}$$

where M is the avalanche multiplication factor, I_{DS} is the drain current of MOSFET, and I_C is

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the collector current of parasitic bipolar transistor. Throughout the simulations, we assumed M=1.1 and "gain" for "G_{gen} in Fig. 2(a) is 0.1.

(iii) Base resistance (RB) of parasitic bipolar transistor is defined as

$$\mathrm{RB} \approx \rho \frac{(L_{eff} - 2x_d)}{T_{si} W}, \quad (3)$$

where x_d is the depletion layer width of the junction.

(iv) Substrate resistance (R_{SUB}) is defined as

$$R_{SUB} = \rho \frac{(L_{eff} + L_D + I_S)}{t \cdot W}. \quad (4)$$

where t is the substrate thickness and ρ is the resistivity.

(v) Gain (BF) of parasitic bipolar transistor is defined as

$$BF = \beta_0 - \Delta\beta_{L_{eff}} \cdot L_{eff} - \Delta\beta_{L_{ld}} \cdot L_{ld} - \Delta\beta_{t_{si}} \cdot t_{si} - \Delta\beta_N \ln\left(\frac{N_A}{N_{ref}}\right), \quad (5)$$

where β_0, β_{tsi}, β_{Leff}, β_{Lld}, β_N and N_{ref} are constants independent of physical parameters.

(vi) Parameter-dependent shift value of the breakdown voltage (V_{BD}) of SOI MOSFET is defined as

$$\Delta V_{BD} = \delta V_{BD0} + \delta\varepsilon_{BDL_{eff}} \cdot L_{eff} + \delta\varepsilon_{BOL_{ld}} \cdot L_{ld} - \delta\varepsilon_{BDt_{si}} \cdot t_{si} - \delta\varepsilon_{BDt_{ox}} \cdot t_{ox} - \delta v_{BDN} \cdot \ln\left(\frac{N_A}{N_{ref}}\right), \quad (6)$$

where δV_{BD0}, $\delta\varepsilon_{BDLeff}$, $\delta\varepsilon_{BDLld}$, $\delta\varepsilon_{BDtsi}$, $\delta\varepsilon_{BDtox}$ and δv_{BDN} are constants independent of physical parameters.

(vii) Parameter-dependent shift value of the holding voltage (V_{SB}) of SOI MOSFET is defined as

$$\Delta V_{SB} = \delta V_{SB0} + \delta\varepsilon_{SBL_{eff}} \cdot L_{eff} + \delta\varepsilon_{SBL_{ld}} \cdot L_{ld} - \delta\varepsilon_{SBt_{si}} \cdot t_{si} - \delta\varepsilon_{SBt_{ox}} \cdot t_{ox} - \delta v_{SBN} \cdot \ln\left(\frac{N_A}{N_{ref}}\right). \quad (7)$$

where δV_{SB0}, $\delta\varepsilon_{SBLeff}$, $\delta\varepsilon_{SBLld}$, $\delta\varepsilon_{SBtsi}$, $\delta\varepsilon_{SBtox}$ and δv_{SBN} are constants independent of physical parameters.

Typical values of β_0, δV_{BD0}, δV_{SB0}, and the above constants are summarized in Table III. Since parameter values shown in Table III are not so sensitive to carrier lifetimes, we can adjust their values easily.

Table III. Constant values in simulations

Parameters	Values [unit]	Parameters	Values [unit]
β_0	19	$\delta\varepsilon_{BDtox}$	1.0×106 [Vm^{-1}]
$\Delta\beta_{Leff}$	2.6×10^7 [m^{-1}]	δv_{BDN}	0.04 [V]
$\Delta\beta_{Lld}$	3.0×10^7 [m^{-1}]	δV_{SB0}	0.47 [V]
$\Delta\beta_{tsi}$	0.7×10^7 [m^{-1}]	$\delta\varepsilon_{SBLeff}$	3.2×10^5 [Vm^{-1}]
$\Delta\beta_N$	1.7	$\delta\varepsilon_{SBLld}$	1.0×10^6 [Vm^{-1}]
N_{ref}	1×10^{18} [cm^{-3}]	$\delta\varepsilon_{SBtsi}$	7.3×10^4 [Vm^{-1}]
δV_{BD0}	1.3 [V]	$\delta\varepsilon_{SBtox}$	2.0×10^6 [Vm^{-1}]
$\delta\varepsilon_{BDLeff}$	1.5×10^5 [Vm^{-1}]	δv_{SBN}	0.02 [V]
$\delta\varepsilon_{BDLld}$	1.6×10^5 [Vm^{-1}]	gain	0.1
$\delta\varepsilon_{BDtsi}$	2.2×10^5 [Vm^{-1}]	M	1.1

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5. Conclusion

We proposed a compact equivalent-circuit model of the snap-back phenomenon in ultra-thin SOI MOSFET's. The model can be used in circuit simulations of I/O circuits with ESD-protection devices. The model is simpler than past models, but it successfully reproduces the snap-back operation of ultra-thin SOI MOSFET's. With the aid of many simulations, we also proposed a guideline for snap-back SOI MOSFET device design. Useful parameter-sensitivity equations for device characteristics were also given for practical device designs.

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